DOCUMENT NUMBER AND REVISION
VL-PS-TLM-MT350Z-01 REV. B
(TLM-MT350Z)

DOCUMENT TITLE:
PRELIMINARY SPECIFICATION
OF
LCD MODULE TYPE
MODEL NUMBER: TLM-MT350Z-01

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DOCUMENT REVISION HISTORY 1:

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	A	2007.09.07	First Release.	PHILIP CHENG	RICKY WONG
A	B	2007.12.06	Items 1~6 were updated: 1.)(Page 4, point 1~2) 320x3x234 dots was changed to 320x234 dots. “Support digital 8-bits serial / 24-bits parallel RGB and CCIR601/656 input mode” was changed to “Support digital 8-bits parallel Mono input mode.”. ”wide view” and remark were eliminated. “WV-film” was changed to “SWV(super wide view”. Dot pitch and weight were updated. 2.)(Page 5~9) The drawing, block diagram and interface signals were updated. 3.)(Page 10, table 5) The max. operating temperature was changed from +85ºC to +80ºC. The max. storage temperature was changed from +90ºC to +85ºC. 4.)(Page 12~18, point 5.3~6) Power consumption, timing characteristics of input signals, timing controller timing chart, and SPI register description and timing characteristics were updated. 5.)(Page 20~23, point 8~11) Pixel arrangement, display gray scale reference, optical characteristics and reliability test were updated. 6.)(whole document)The point no., figure no. and table no. were updated.	PHILIP CHENG	RICKY WONG

CONTENTS

VARITRONIX LIMITED

Preliminary Specification
of
LCD Module Type
Model No.: TLM-MT350Z-01

1. General Description

- 3.5"(diagonal), 320 x 234 dots, positive, transmissive, Mono TFT LCD module.
- Viewing angle: 6 o'clock.
- Logic voltage: +3.3V.
- Support digital 8-bits parallel Mono input mode.
- Provide source and gate drivers control timing.
- Image Reversion: Up/Down and Left/Right.
- White LED backlight.
- FPC connection.
- Anti-glare + SWV (super wide view).

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter		Specifications	Unit
Outline dimensions		84.03(W) x 65.24(H) x 3.43(D) (excluded FPC)	mm
Mono TFT 320 x 234	Bezel opening	74.60(W) x 55.65(H)	mm
	Active area	71.60(W) x 52.65(H)	mm
	Display format	320 x 234	dots
	Pixel Configuration	Delta	-
	Dot pitch	0.22375(W) x 0.225(H)	mm
Weight		TBD	grams

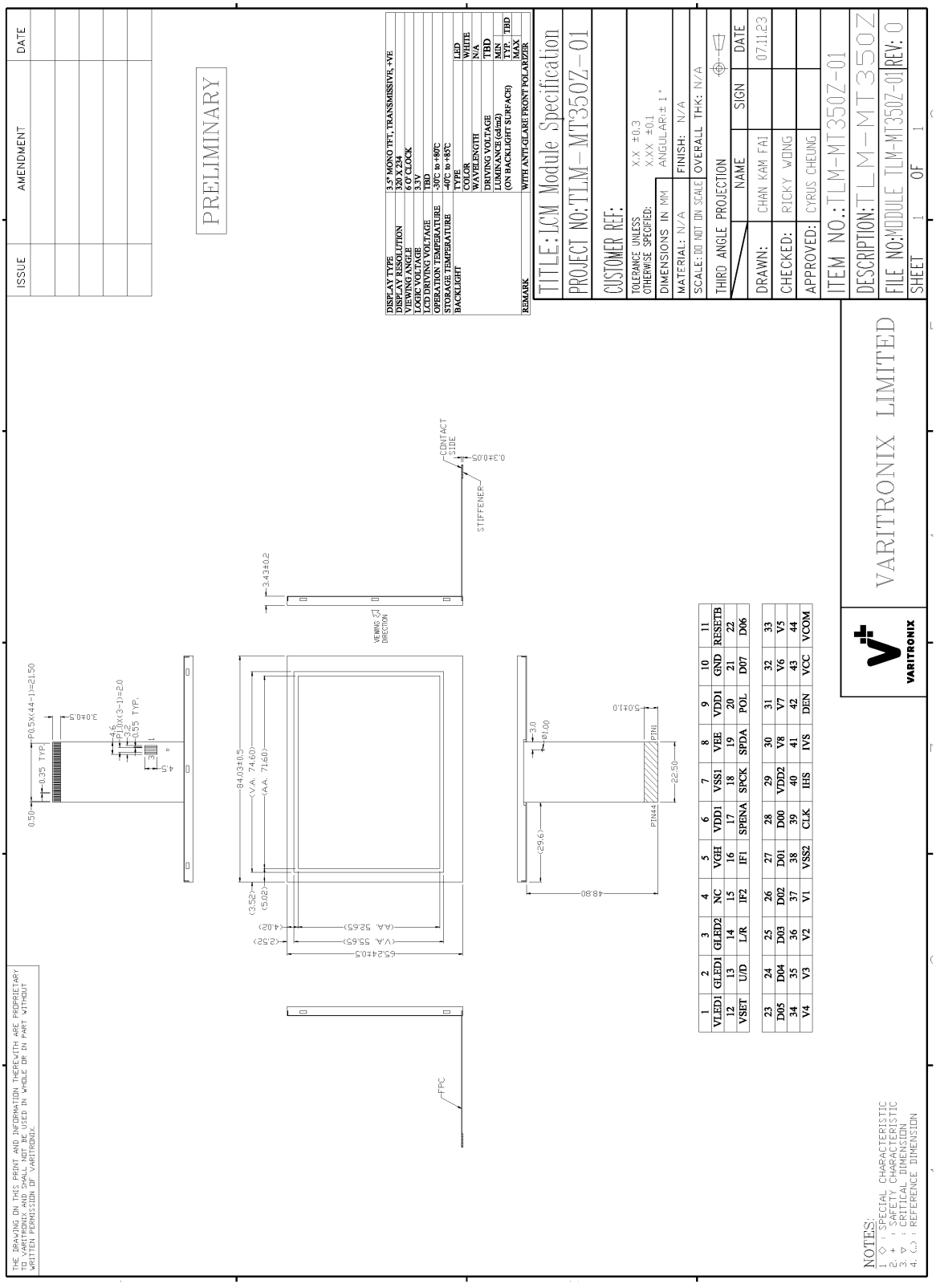


Figure 1: Outline Drawing

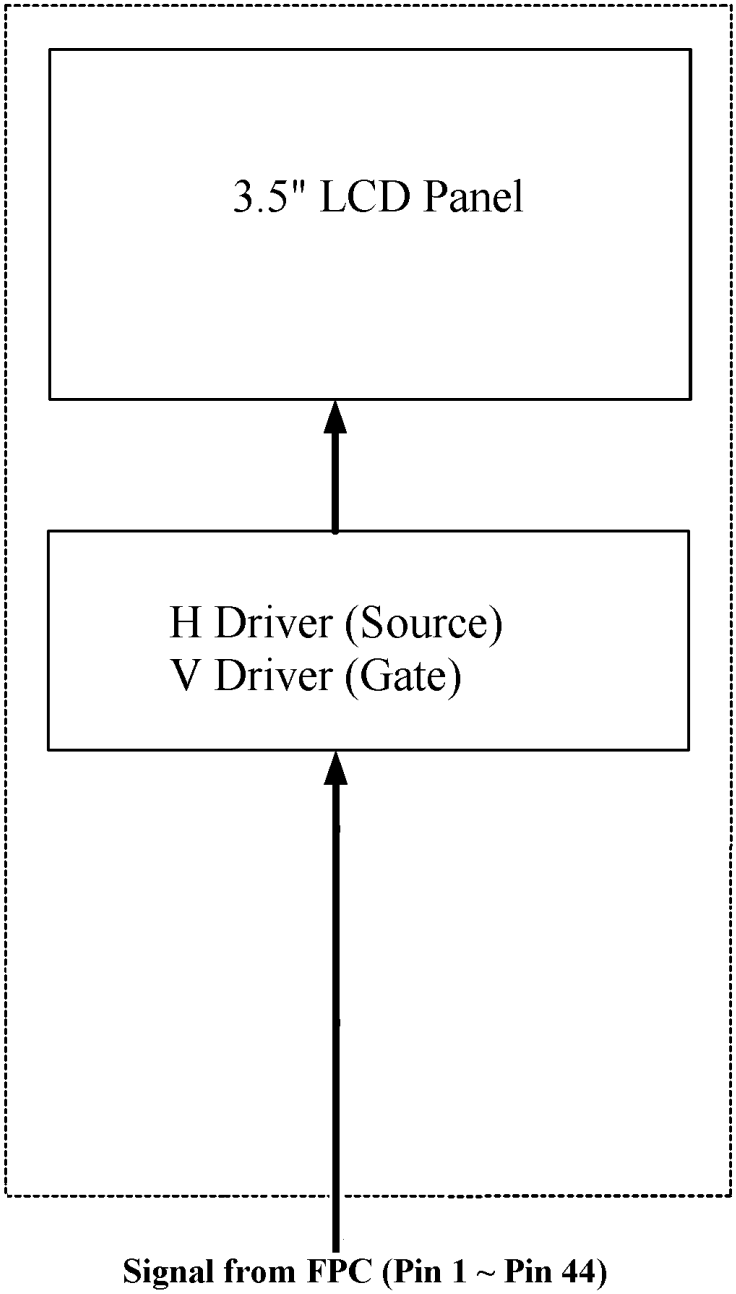


Figure 2: Block Diagram

3. Interface Signals

Table 2(a): Pin assignment

Pin No	Symbol	I/O	Description	Remark
1	VLED1	I	Power supply for LED	
2	GLED1	I	Ground for LED	
3	GLED2	I	Ground for LED	
4	NC	I	NC	
5	VGH	I	Positive power for gate driver	Note 1
6	VDD1	I	Power supply for gate logic circuit	Note 2
7	VSS1	I	Ground for gate driver	
8	VEE	I	Negative power for gate driver	Note 3
9	VDD1	I	Power supply for gate logic circuit	Note 4
10	GND	I	Digital ground for source driver IC	
11	RESETB	I	Hardware global reset, (low active)	
12	VSET	I	Externally/Internally gamma voltage setup	
13	U/D	I	Up/Down control for gate driver	Note 5
14	L/R	I	Left/Right control for source driver	Note 5
15	IF2	I	Ground	Note 6
16	IF1	I	VCC	Note 6
17	SPENA	I	Serial port data enable signal (normally pull high)	
18	SPCK	I	Serial port clock. (Normally pull high)	
19	SPDA	I/O	Serial port data input/output	
20	POL	O	Polarity select for the line inversion control signal	Note 7
21	D07	I	Data Input	
22	D06	I	Data Input	
23	D05	I	Data Input	
24	D04	I	Data Input	
25	D03	I	Data Input	
26	D02	I	Data Input	
27	D01	I	Data Input	
28	D00	I	Data Input	
29	VDD2	I	Analog power supply for source driver	Note 8
30	V8	I	Gamma correction voltage 8	Note 9
31	V7	I	Gamma correction voltage 7	
32	V6	I	Gamma correction voltage 6	
33	V5	I	Gamma correction voltage 5	
34	V4	I	Gamma correction voltage 4	
35	V3	I	Gamma correction voltage 3	
36	V2	I	Gamma correction voltage 2	
37	V1	I	Gamma correction voltage 1	
38	VSS2	I	Analog ground for source driver	
39	CLK	I	Clock signal. Latching data at the rising edge	

Table 2(b): Pin assignment

Pin No	Symbol	I/O	Description	Remark
40	IHS	I	Horizontal sync input.	Note 10
41	IVS	I	Vertical sync input.	Note 11
42	DEN	I	Input data enable control.(Normally pull low)	Note 12
43	VCC	I	Digital power supply for source driver IC	Note 13
44	VCOM	I	Voltage for common electrode	Note 14

Note 1: VGH Typ. =+15V.

Note 2: VDD1 Typ.＝+3.3V.

Note 3: VEE Typ. = -15V.

Note 4: VDD1 Typ.＝+3.3V.

Note 5:

U/D(PIN 20)=Low L/R(PIN 15)=High U/D(PIN 20)=High L/R(PIN 15)=Low

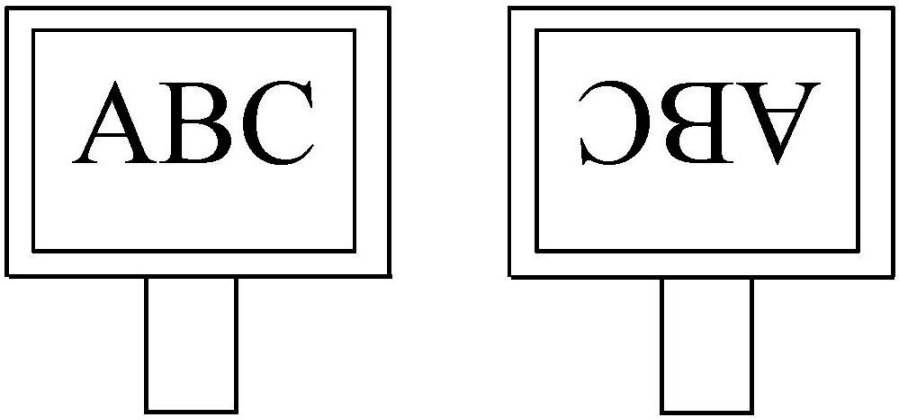


Figure 3

Note 6: IF1=Ground and IF2=VCC.

Note 7:When POL=L, output voltage is negative polarity.
When POL=H, output voltage is positive polarity.

Note 8: VDD2 Typ. = +5V.

Note 9 : The output voltage is determined by the digital input data. The 8 gamma correction reference voltages can be set to externally or generate internally.
If VSET = ”H”, the gamma correction voltage generated externally
If VSET = “L”, the default value is as below: (When VDD=+5V)

Table 3

	V1	V2	V3	V4	V5	V6	V7	V8
Default Voltage(V)	4.29	3.73	3.33	2.94	2.62	2.22	1.51	0.48

Note 10 : Horizontal sync input. (Short to VSS if not used)

Note 11 : Vertical sync input . (Short to Vss if not used)

Note 12 : For digital parallel input data format, both SYNC. Mode and DEN mode are supported. If DEN signal is fixed low, SYNC. Mode is used. Otherwise, DEN mode is used.

Note 13 : VCC Typ. = +3.3V.

Note 14 : VCOM Typ.＝+6.0Vpp.

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings – For IC Only

Table 4

Parameters		Symbol	MIN.	MAX.	Unit	Remark
Supply voltage for source driver		VCC	-0.3	+7.0	V	
		VDD2	-0.3	+7.0	V	
Supply voltage for gate driver		VDD1	-0.3	+7.0	V	
	H level	VGH	-0.3	+32.0	V	
	L level	VEE	-22.0	+0.3	V	
		VGH-VEE	-0.3	+45.0	V	
Input signal voltage		VIN	-0.3	VDD+0.3	V	

Note: 1. The modules may be destroyed if they are used beyond the absolute maximum ratings.
2. VSS1=VSS2=0V, Ta=25°C.

4.2 Environmental Condition

Table 5

Item	Operating temperature (Topr)		Storage temperature (Tstg) (Note 1)		Remark
	Min.	Max.	Min.	Max.	
Ambient temperature	-30°C	+80°C	-40°C	+85°C	Dry

Note 1: Product cannot sustain at extreme storage conditions for long time.

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VCC=VDD1=3.3V±0.3V, VSS1=VSS2=0V.

Table 6

Parameter		Symbol	MIN.	Typ.	MAX.	Unit	Remark
Supply voltage for source driver	Logic	VCC	+3.0	+3.3	+3.6	V	
	Analog	VDD2	+3.8	+5.0	+5.5	V	
Supply voltage for gate driver	Logic	VDD1	+3.0	+3.3	+3.6	V	
	H level	VGH	+10	+15	+30	V	
	L level	VEE	-17	-15	-5	V	
Signal input voltage	H level	VIH	0.7VCC	-	VCC	V	
	L level	VIL	0	-	0.3VCC	V	
Signal output voltage	H level	VoH	0.8VCC	-	VCC	V	
	L level	VoL	0	-	0.2VCC	V	
VCOM		VCOMAC	-	+6.0	-	V_{P-P}	AC Component of VCOM
		VCOMDC	-	1.0	-	V	DC Component of VCOM Note 1

Note 1: The VCOMDC level shall be adjustable, and the adjustable level range is 1V±1V, every module's VCOMDC level shall be carefully adjusted to show a best image performance.

5.2 Recommended Driving Condition For LED Backlight

Table 7

Parameter	Symbol	Min	TYP	MAX	Unit	Remark
Supply voltage of LED backlight	VLED	9.0	10.0	11.0	V	I_L = 20 mA
Supply current of LED backlight	ILED	-	20	-	mA	Note 1
Backlight Power Consumption	PLED	360	400	440	mW	Note 2

Note 1: LED B/L applied information, please refer to the below reference.

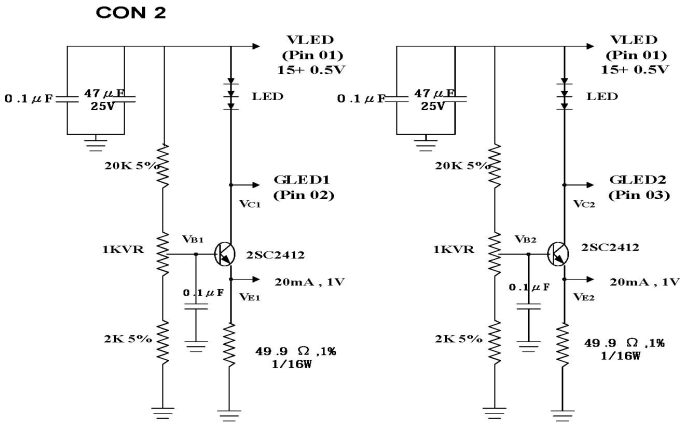


Figure 4

Note 2: $P_{LED} = 2*I_{LED}*V_{LED}$.

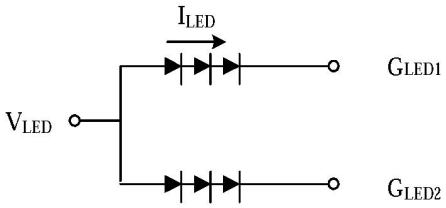


Figure 5

5.3 Power Consumption

Table 8 (VSS1=VSS2=0 V, Ta = 25°C)

Parameter	Symbol	Conditions	TYP.	MAX.	Unit	Remark
Supply current for gate driver (Hi level)	IGH	VGH=+15V	0.2	0.6	mA	
Supply current for gate driver(Logic)	IDD1	VDD1=+3.3V	0.1	0.3	mA	
Supply current for gate driver (Low level)	IEE	VEE=-15V	0.2	0.6	mA	VEE center voltage
Supply current for source driver(Analog)	IDD2	VDD2=+5V	5.0	10.0	mA	
Supply current for source driver(Logic)	ICC	VCC=+3.3V	4.5	9.0	mA	
LCD panel power consumption	-		46.18	98.69	mW	
Backlight power consumption	P_{LED}		400	440	mW	
Total power consumption	-		0.45	0.54	W	

5.4 Timing Characteristics Of Input Signals

5.4.1 Parallel 8 Bits Interface

Table 9

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
CLK period	T_{OSC}	-	156	-	ns	Note 1
Data setup time	T_{SU}	12	-	-	ns	
Data hold time	T_{HD}	12	-	-	ns	
HS period	T_{H}	-	408	-	T_{OSC}	
HS pulse width	T_{HS}	5	30	-	T_{OSC}	
HS rising time	T_{Cr}	-	-	700	ns	
HS falling time	T_{Cf}	-	-	300	ns	
VS pulse width	T_{VS}	1	3	5	T_{H}	
VS rising time	T_{Vr}	-	-	700	ns	
VS falling time	T_{Vf}	-	-	1.5	us	
HS falling to VS falling time for odd field	T_{HVO}	0	3	-	T_{OSC}	
VS falling to HS falling time for even field	T_{HVE}	0	3	-	T_{OSC}	
VS-DEN time	T_{VSE}	-	18	-	T_{H}	
HS-DEN time	T_{HE}	36	68	88	T_{OSC}	
DEN pulse width	T_{EP}	-	320	-	T_{OSC}	
VS period		-	262	-	T_{H}	

Note 1: When SYNC mode is used, 1st data start from 68th CLK after HS fallings.

5.5 Timing Controller Timing Chart

5.5.1 HS,VS,DEN Timing Waveform

5.5.1.1 HS And VS Timing Relationship

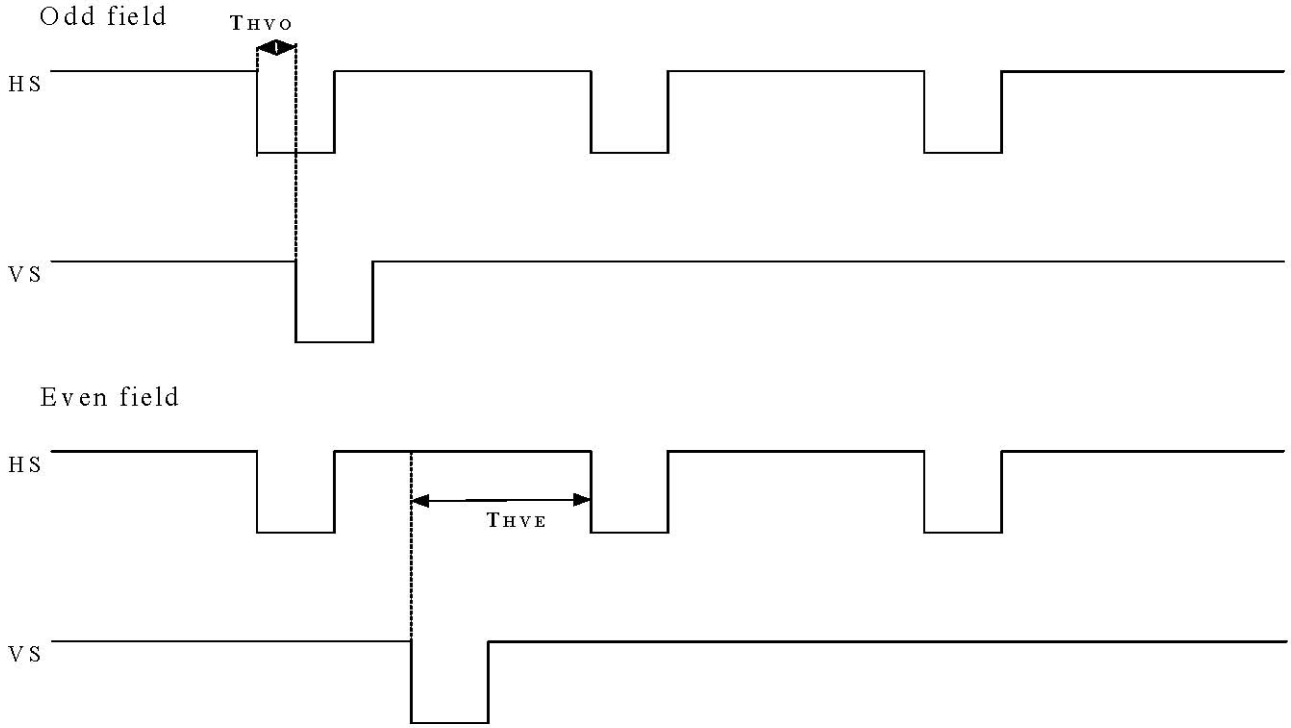


Figure 6

5.5.1.2 HS And DEN Timing Relationship

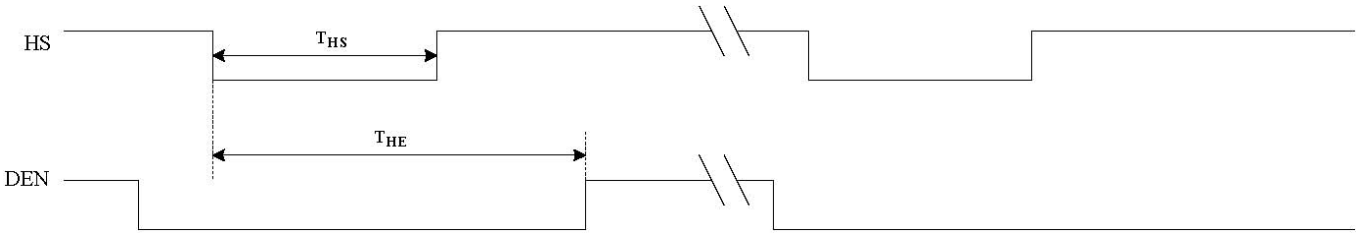


Figure 7

5.5.1.3 HS, VS And DEN Timing Relationship

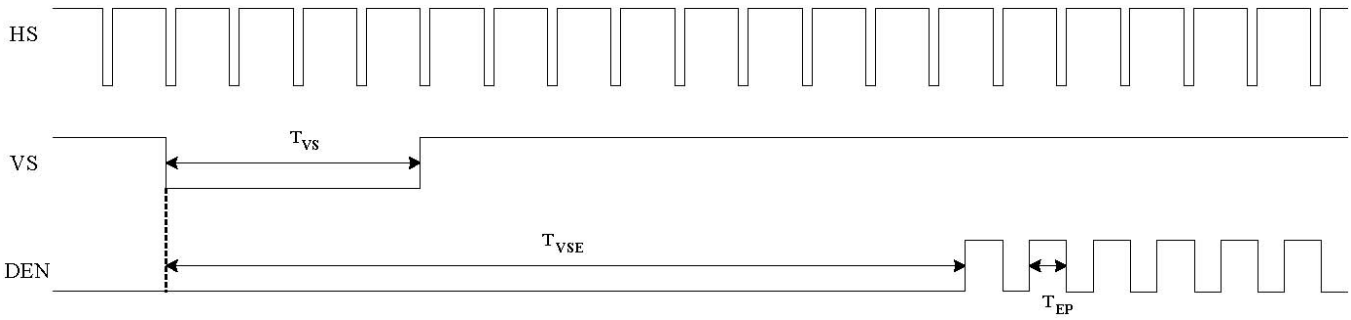


Figure 8

6. SPI Register Description and Timing Characteristics

6.1 Function Control Register

6.1.1 Register R0 :Address(A3~A0)→0000

Table 10

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	STHD1	STHD0	STHP4	STHP3	STHP2	STHP1	STHP0
Default	0	0	0	0	0	0	0	0

Table 11: STHD [1:0] : adjust start pulse position by dot

STHD1	STHD0	STH position adjust by dot
1	1	-1
1	0	-2
0	0	0
0	1	+1

Table 12(a): STHP [4:0] : adjust start pulse position by pixel

STHP4	STHP3	STHP2	STHP1	STHP0	STH position adjust by pixel
1	1	1	1	1	-1
1	1	1	1	0	-2
1	1	1	0	1	-3
1	1	1	0	0	-4
1	1	0	1	1	-5
1	1	0	1	0	-6
1	1	0	0	1	-7
1	1	0	0	0	-8
1	0	1	1	1	-9
1	0	1	1	0	-10
1	0	1	0	1	-11
1	0	1	0	0	-12
1	0	0	1	1	-13
1	0	0	1	0	-14
1	0	0	0	1	-15
1	0	0	0	0	-16
0	0	0	0	0	0
0	0	0	0	1	+1
0	0	0	1	0	+2
0	0	0	1	1	+3
0	0	1	0	0	+4
0	0	1	0	1	+5
0	0	1	1	0	+6
0	0	1	1	1	+7
0	1	0	0	0	+8
0	1	0	0	1	+9

Table 12(b): STHP [4:0] : adjust start pulse position by pixel

STHP4	STHP3	STHP2	STHP1	STHP0	STH position adjust by pixel
0	1	0	1	0	+10
0	1	0	1	1	+11
0	1	1	0	0	+12
0	1	1	0	1	+13
0	1	1	1	0	+14
0	1	1	1	1	+15

6.1.2 Register R1 :Address(A3~A0)→0001

Table 13

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	STVP3	STVP2	STVP1	STVP0	STVNT1	STVNT0	STVPAL1	STVPAL0
Default	0	0	0	0	0	0	0	1

Table 14: STVP [3:0] : adjust first line position by line

STVP3	STVP2	STVP1	STVP0	STV position adjust by line
1	1	1	1	-1
1	1	1	0	-2
1	1	0	1	-3
1	1	0	0	-4
1	0	1	1	-5
1	0	1	0	-6
1	0	0	1	-7
1	0	0	0	-8
0	0	0	0	0
0	0	0	1	+1
0	0	1	0	+2
0	0	1	1	+3
0	1	0	0	+4
0	1	0	1	+5
0	1	1	0	+6
0	1	1	1	+7

STVNT[1:0]: When NTSC mode, the relationship of first line in Even field and Odd field.

00: First line in Even field = First line in Odd field.

01: First line in Even field = First line in Odd field +1.

10: No use.

11: First line in Even field = First line in Odd field –1.

STVPAL[1:0]: When PAL mode, the relationship of first line in Even field and Odd field.
(Only for CCIR601/656 mode)
00: First line in Even field = First line in Odd field.
01: First line in Even field = First line in Odd field +1.
10: No use.
11: First line in Even field = First line in Odd field –1.

6.1.3 Register R2 :Address(A3~A0)→0010

Table 15

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	reserved	reserved	HS_POL	VS_POL	NPC_IN	NPC_SET
Default	0	0	0	1	0	0	1	0

HS_POL: HS polarity setting.
HS_POL = “L”, negative polarity.
HS_POL = “H”, positive polarity.
VS_POL: VS polarity setting.
VS_POL = “L”, negative polarity.
VS_POL = “H”, positive polarity.
NPC_IN: Define the NTSC/PAL mode by SPI.
NPC_IN = “L”, PAL. (Only for CCIR601/656 mode)
NPC_IN = “H”, NTSC.
NPC_SET: Set the NTSC/PAL auto detection or define by NPC_IN.
NPC_SET = “L”, auto detection.
NPC_SET = “H”, define by SPI.

6.1.4 Register R3 :Address(A3~A0)→0011

Table 16

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	reserved	reserved	reserved	reserved	PWD_EN	reserved	reserved	reserved
Default	0	0	1	0	1	0	1	1

PWD_EN: Set DAC power saving function.
PWD_EN = “L”, disable. The DAC is always power on.
PWD_EN = “H”, enable.

6.2 SPI Timing Characteristic

Table 17

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Remark
SPCK period	T_{CK}	60	-	-	ns	
SPCK high width	T_{CKH}	30	-	-	ns	
SPCK low width	T_{CKL}	30	-	-	ns	
Data setup time	T_{SU1}	12	-	-	ns	
Data hold time	T_{HD1}	12	-	-	ns	
SPENA to SPCK setup time	T_{CS}	20	-	-	ns	
SPENA to SPDA hold time	T_{CE}	20	-	-	ns	
SPENA high pulse width	T_{CD}	50	-	-	ns	
SPDA output latency	T_{CR}	-	1/2	-	T_{CK}	

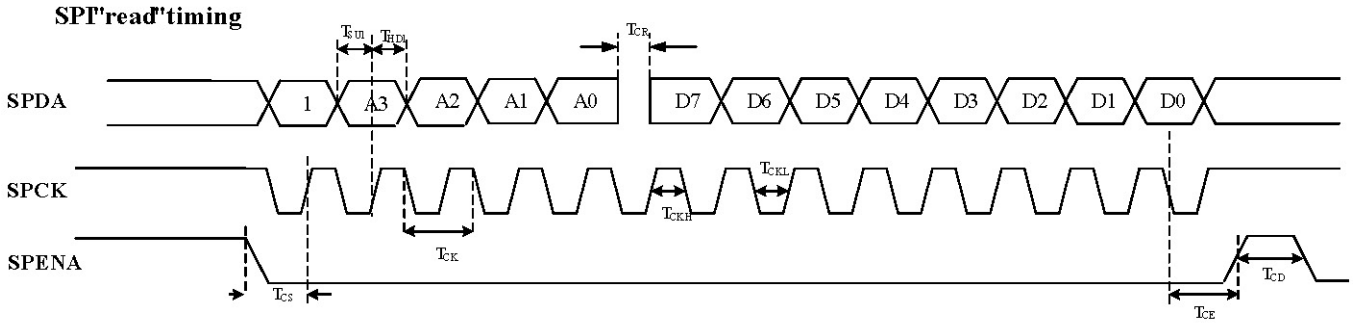


Figure 9: SPI "read" timing

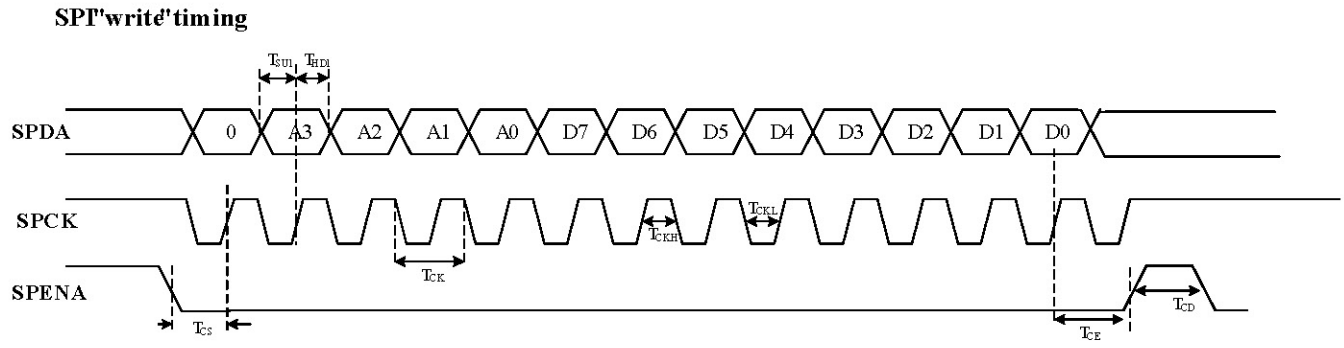
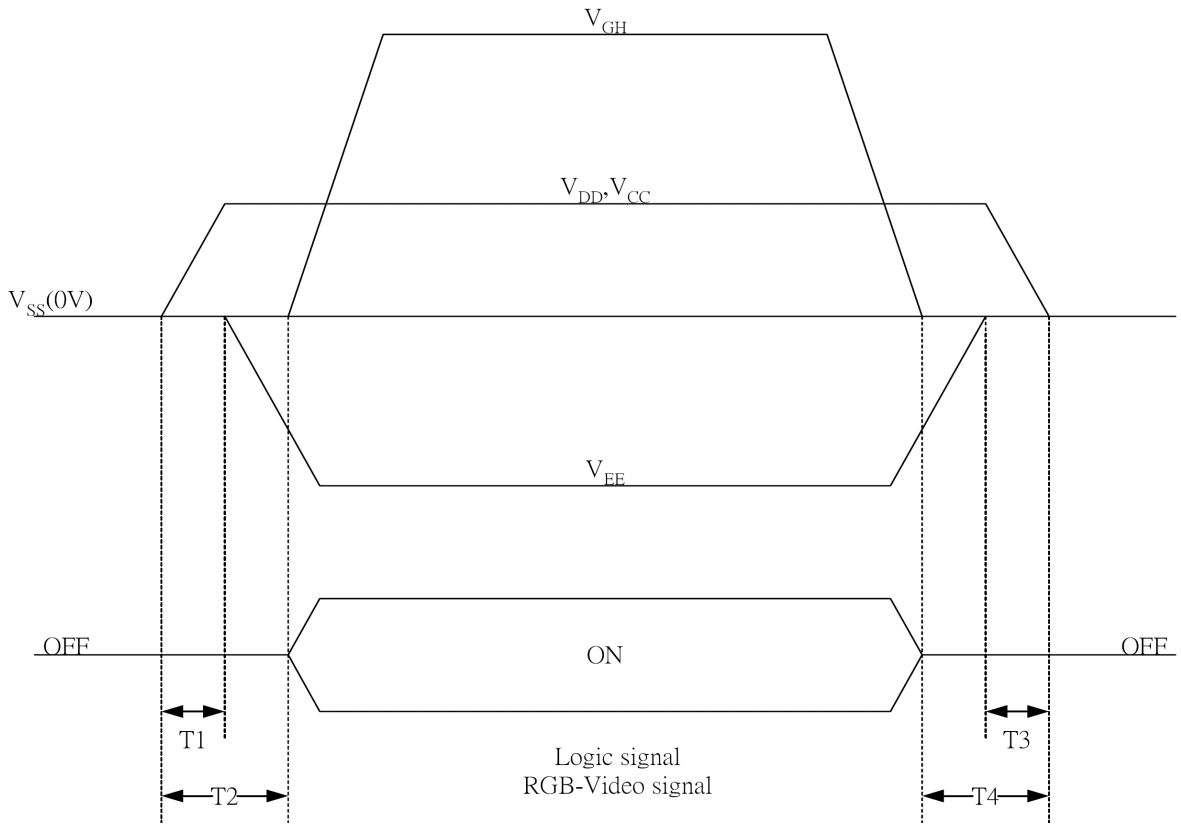


Figure 10: SPI "write" timing

7. Power On Sequence

The Power on sequence only effect by V_{CC},V_{SS},V_{DD},V_{EE} and $V_{GH,}$ the others do not care.



1) 10ms≦T1<T2

2) 0ms<T3≦T4≦10ms

Figure 11

8. Pixel Arrangement

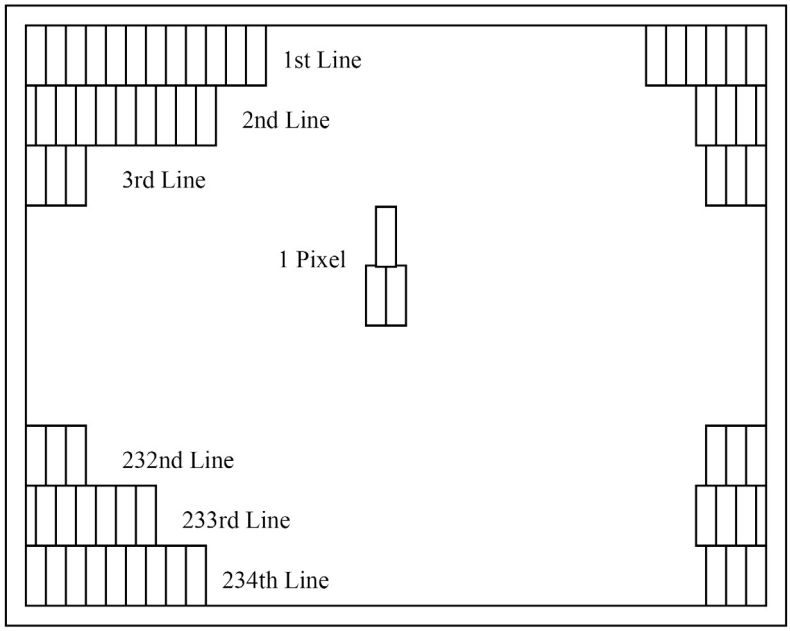


Figure 12

9. Display Gray Scale Reference

Table 18

Data		Input Data							
		Gray							
		D7	D6	D5	D4	D3	D2	D1	D0
Gray	000	0	0	0	0	0	0	0	0
	001	0	0	0	0	0	0	0	1
	002	0	0	0	0	0	0	1	0
	↓	↓	↓	↓	↓	↓	↓	↓	↓
	254	1	1	1	1	1	1	0	1
	255	1	1	1	1	1	1	1	0
	256	1	1	1	1	1	1	1	1

10. Optical Characteristics

Table 19: Optical characteristics (Ta=25°C)

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing angle	Horizontal	ϕ1(3 o'clock), ϕ2(9 o'clock)	CR≧TBD	-	TBD	-	Deg	Note 1
	Vertical	θ1(6 o'clock)		-	TBD	-	Deg	
		θ2(12 o'clock)		-	TBD	-	Deg	
Contrast ratio		CR	At optimized Viewing angle	-	TBD	-		Note 2
Cross talk			θ=0°, ϕ=0°	-	-	3.5	%	Note 4
Transmission ratio				-	TBD	-	%	
Response time	Rise	Tr	θ=0°, ϕ=0°	-	TBD	-	ms	Note 3
	Fall	Tf		-	TBD	-	ms	

Note 1: The definitions of viewing angles

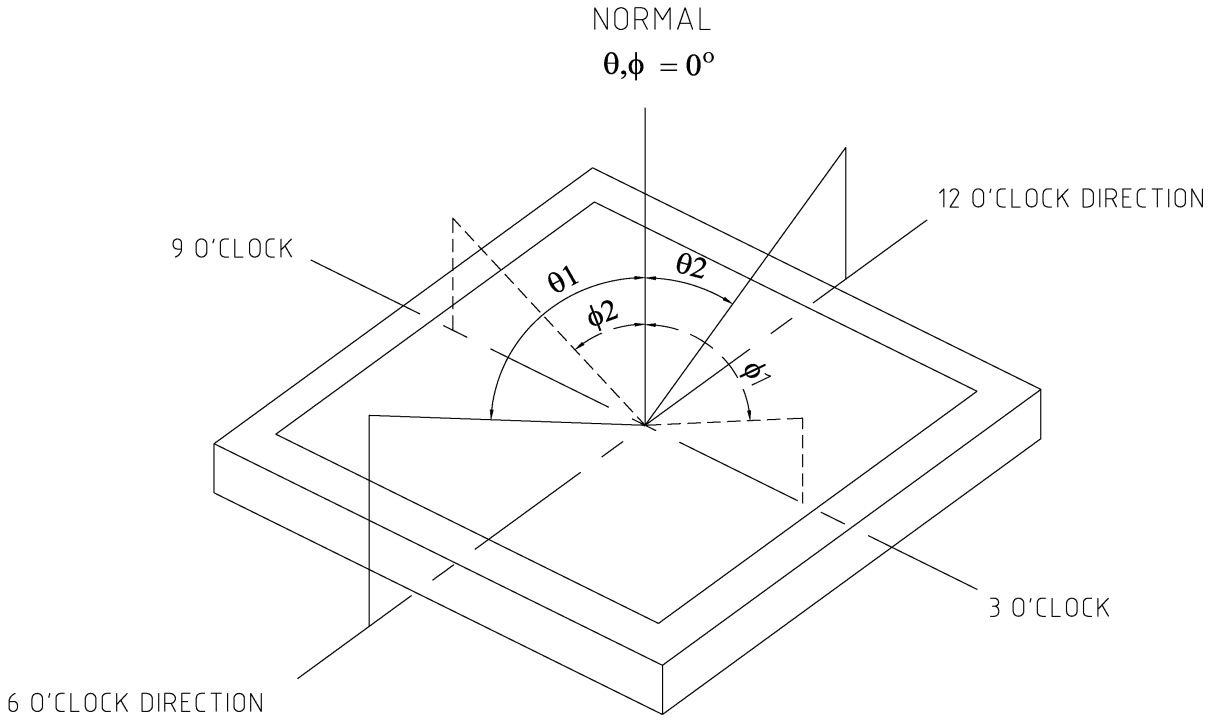


Figure 13

Note 2 : CR = $\frac{\text{Luminance when Testing point is White}}{\text{Luminance when Testing point is Black}}$

Contrast ratio is measured in optimum common electrode voltage.

Note 3: The definition of response time :

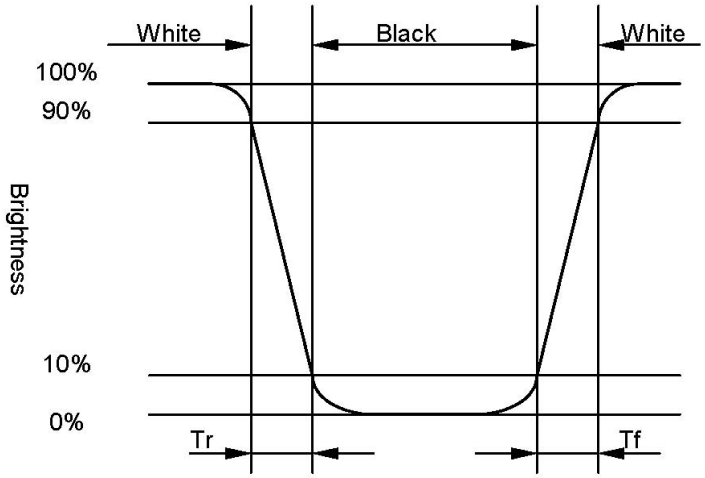


Figure 14

Note 4 : Test configuration:

$$\text{Crosstalk(CTK)} = \frac{|YA-YB|}{TA} \times 100\%$$

YA: Brightness of Pattern A

YB: Brightness of Pattern B

Luminance meter : BM-5A or BM-7 fast (TOPCON)

Measurement distance : 500 mm +/- 50 mm

Ambient illumination : < 1 Lux

Measuring direction : Perpendicular to the surface of module

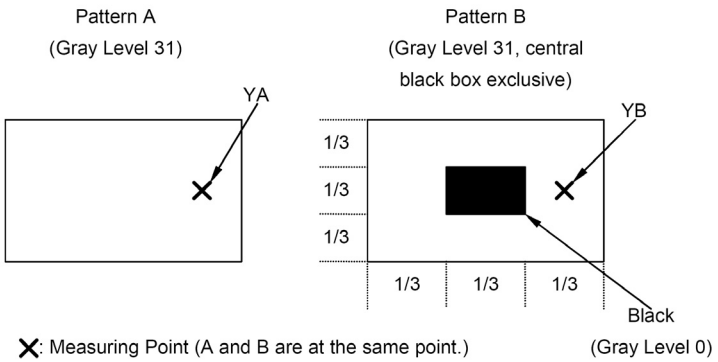


Figure 15

11. Reliability Test

Table 20

No	Test Item	Test Condition
1	High Temperature Storage Test	Ta=+85°C, 240hrs
2	Low Temperature Storage Test	Ta =-40°C, 240 hrs
3	High Temperature Operation Test	Ta = +80°C, 240 hrs
4	Low Temperature Operation Test	Ta = -30°C, 240 hrs
5	High Temperature & High Humidity Operation Test	Ta = +70°C, 90%RH, 240 hrs
6	Thermal Cycling Test (non-operating)	-20°C ⟷ +70°C, 200 Cycles 30 min 30 min
7	Electrostatic Discharge Test (non-operating)	200pF, 0Ω Machine mode = ±200V 1 time / each terminal

Ta: ambient temperature

[Criteria]

In the standard conditions, there is not display function NG issue occurred. (Including：line defect ,no image) All the cosmetic specification is judged before the reliability stress.

12. Handling Cautions

12.1 Mounting Of Module

- Please power off the module when you connect the input/output connector.
- If the backlight connection is not perfect, some following problems may happen possibly.
  1. The noise from the backlight unit will increase.
  2. The backlight performance will be unstable.
  3. In some cases a part of module will heat.
- Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
- Protective film (Laminator) is applied on surface to protect it against scratches and dirt. It is recommended to peel off the laminator before use and taking care of static electricity.

12.2 Precautions In Mounting

- When metal part of the TFT-LCD module (shielding lid and rear case) is soiled,wipe it with soft dry cloth.
- Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
- TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
- Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

12.3 Adjusting module

- Adjusting volumes on the rear face of the module have been set optimally before shipment.
- Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

12.4 Others

- Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.
- Store the module at a room temperature place.
- If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
- Observe all other precautionary requirements in handling general electronic components.
- Please adjust the voltage of common electrode as material of attachment by 1 module.

12.5 Polarizer mark

-The polarizer mark is to describe the direction of wide view angle film how to mach up with the rubbing direction.